

Video Sync Generator

032

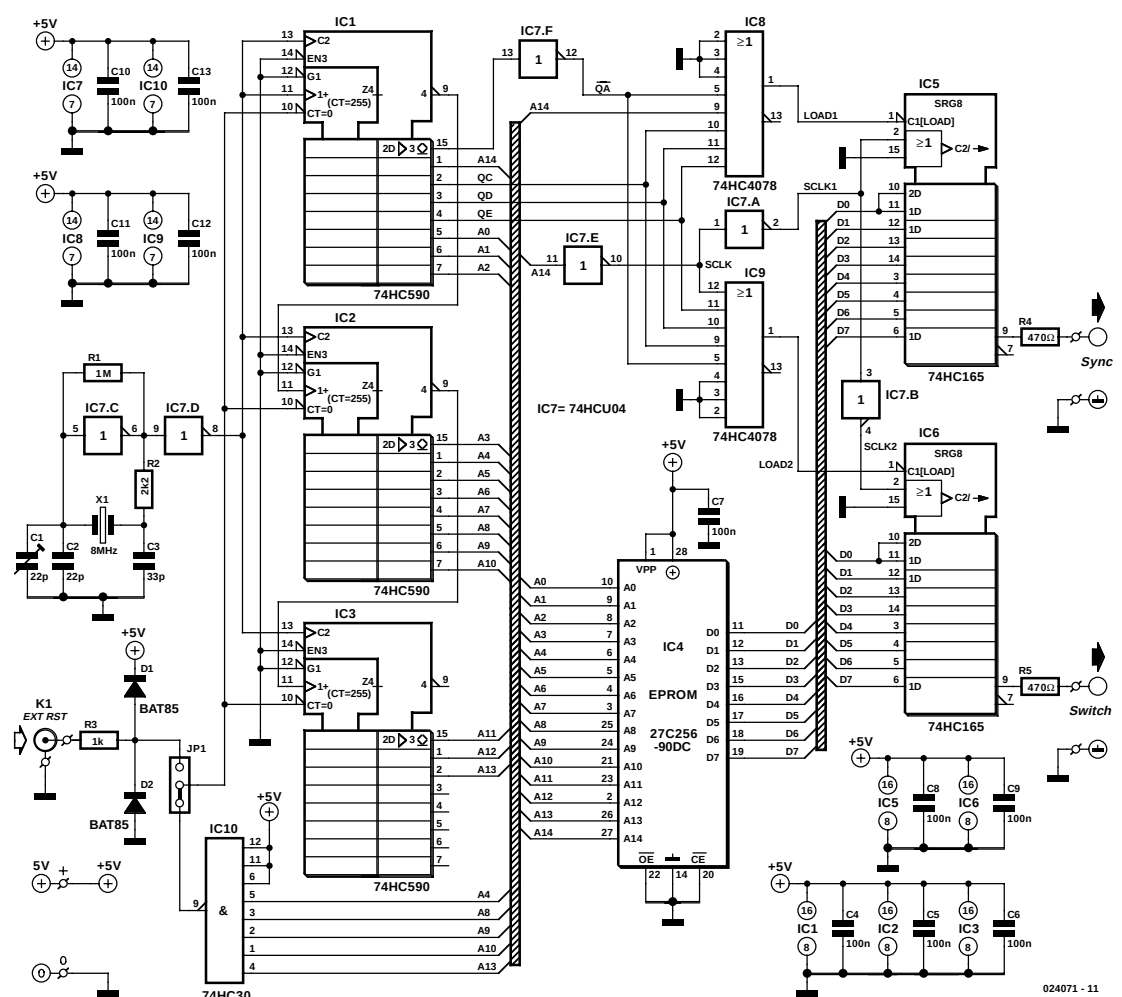
Special ICs, such as the Fairchild 74ACT715 (formerly National LM1882) and the Philips SAA1001, have been developed for generating video synchronisation signals. However, the annoying thing about such ICs is that they are often difficult to obtain. On top of that, there are other problems, such as that the one has to be initialised by a processor and the other is difficult to synchronise to an external signal or ends up being incorrectly synchronised. However, it is also possible to use a 'discrete' circuit to generate the video sync signal for a project such as a homemade test pattern generator.

In the design described here, we assume a field rate of

50 Hz and a horizontal line rate of 15,625 Hz. Our solution is based on using an EPROM containing a 'sampled' version of the signal. A second table is also programmed for operating a video switch. If you can program the EPROM yourself, you can modify the second table to produce a black-level clamping signal or generate a simple monochrome test pattern, among other possibilities.

The circuit is designed to make it easy to view and modify the content of the EPROM using a hex editor. Each video line is constructed from the data contained in 16 successive data bytes. If the hex editor always displays 16 bytes per line, you can 'view' the video lines as they actually are (in hexadecimal form, of course).

With the exception of the EPROM, the circuit consists of only standard logic devices. The 15-bit address for the EPROM is generated by three synchronous counters (IC1–IC3) connected in series. In order to allow the two tables in the EPROM to be clearly distinguished, the highest address line (A14) is switched 16 times faster than the A0 line. This means that the



two tables in the EPROM are located one above the other, rather than interleaved. This makes it much easier to modify the second table for your own applications.

The counters are clocked by a standard 8-MHz crystal oscillator (built using IC7c, a 74HCU04 buffer). The first counter (IC1) and its output register are clocked by the oscillator. The

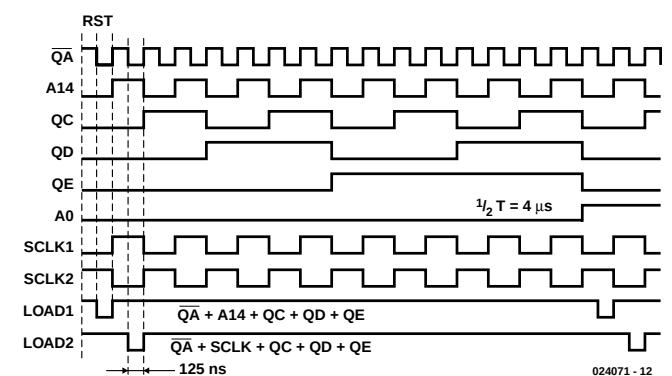


Table 1

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0000h: 00 00 00 00 00 00 01 FF 00 00 00 00 00 01 FF
0010h: 00 00 00 00 00 00 01 FF 00 00 00 00 00 01 FF
0020h: 00 00 00 00 00 00 01 FF 07 FF FF FF FF FF FF
0030h: 07 FF FF FF FF FF FF 07 FF FF FF FF FF FF
0040h: 07 FF FF FF FF FF FF 07 FF FF FF FF FF FF
0050h: 00 7F FF FF FF FF FF FF FF FF FF FF FF FF
0060h: 00 7F FF FF FF FF FF FF FF FF FF FF FF FF
1340h: 00 7F FF FF FF FF FF FF FF FF FF FF FF FF
1350h: 00 7F FF FF FF FF FF FF FF FF FF FF FF FF
1360h: 07 FF FF FF FF FF FF 07 FF FF FF FF FF FF
1370h: 07 FF FF FF FF FF FF 07 FF FF FF FF FF FF
1300h: 07 FF FF FF FF FF FF 00 00 00 00 00 01 FF
1390h: 00 00 00 00 00 01 FF 00 00 00 00 00 01 FF
13A0h: 00 00 00 00 00 01 FF 00 00 00 00 00 01 FF
13B0h: 07 FF FF FF FF FF FF 07 FF FF FF FF FF FF
13C0h: 07 FF FF FF FF FF FF 07 FF FF FF FF FF FF
13D0h: 07 FF FF FF FF FF FF FF FF FF FF FF FF
13E0h: 00 7F FF FF FF FF FF FF FF FF FF FF FF
13F0h: 00 7F FF FF FF FF FF FF FF FF FF FF FF
26C0h: 00 7F FF FF FF FF FF FF FF FF FF FF FF
26D0h: 00 7F FF FF FF FF FF FF FF FF FF FF FF
26E0h: 00 7F FF FF FF FF FF 07 FF FF FF FF FF FF
26F0h: 07 FF FF FF FF FF FF 07 FF FF FF FF FF FF
2700h: 07 FF FF FF FF FF FF 07 FF FF FF FF FF FF
2710h: F0 00 00 00 00 00 00 00 00 00 00 00 00
2720h: 00 00 00 00 00 00 00 00 00 00 00 00 00
2730h: 00 00 00 00 00 00 00 00 00 00 00 00 00

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second counter (IC2) is clocked by the ripple-carry output of the previous counter, with its output register being clocked by the oscillator. The same applies to the third counter (IC3), with the result that the outputs of the counter ICs change state simultaneously. This is necessary to have the data on the EPROM outputs become stable as quickly as possible.

The data from the EPROM are converted into the actual video waveform by two shift registers (IC5 and IC6, which are 8-bit PISO types). The timing diagram shows how all of this works for a single byte. The correct control signals for the shift registers are formed from the first counter outputs of IC1 using a bit of logic. The Load1 signal (IC8) loads the data for the synchronisation signal into IC5. At this point, A14 is Low and data from the first table are present at the EPROM outputs. After this, the Load2 signal (IC9) performs the same function for the data from the second table (A14 High), and IC6 provides the signal for a video switch (or something else). Inverters IC7a and IC7b ensure that the data in the shift registers are clocked through at the correct time. Note that IC8 and IC9 must have a non-inverting output (pin 1); the original 4078 from the standard CMOS family has only an inverting output. Here we have used Texas Instruments types. If a non-inverting output is not available, two additional inverters will naturally be needed.

IC10 is used to reset the counters at the end of line 625. This occurs after 10,000 bytes (16×625), or 80,000 bits. The resolution is thus $0.05 \mu\text{s}$, with each line consisting of 128 samples. For the sake of completeness, we should note that the signal at the output of IC6 lags the signal at the output of IC5 by $0.25 \mu\text{s}$, but this does not have any practical consequences. A fast (90 ns) EPROM from AMD is used here, since the data must be transferred to the shift registers within 125 ns, and this time is further reduced by the various propagation delays.

If jumper JP1 is placed in the upper position, an externally

Table 2

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4000h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4010h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4020h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4030h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4040h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4050h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
4060h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
4070h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
4080h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
4090h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
40A0h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
40B0h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
40C0h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
40D0h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
40E0h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
40F0h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
4100h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
4110h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
4120h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
4130h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
4140h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
4150h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
4160h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
4170h: 00 3F 87 FF FF FF FF FF FF FF FF FF FF FF
4180h: 00 3F 87 FF FF FF FF FF FF FF FF FF FF FF
5340h: 00 3F 87 FF FF FF FF FF FF FF FF FF FF FF
5350h: 00 3F 87 FF FF FF FF FF FF FF FF FF FF FF
5360h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
5370h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
5380h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
5390h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
53A0h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
53B0h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
53C0h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
53D0h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
53E0h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
53F0h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
5400h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
5410h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
5420h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
5430h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
5440h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
5450h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
5460h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
5470h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
5480h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
5490h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
54A0h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
54B0h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
54C0h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
54D0h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
54E0h: 00 3F 80 00 00 00 00 00 00 00 00 00 00 00
54F0h: 00 3F 87 FF FF FF FF FF FF FF FF FF FF FF
5500h: 00 3F 87 FF FF FF FF FF FF FF FF FF FF FF
66C0h: 00 3F 87 FF FF FF FF FF FF FF FF FF FF FF
66D0h: 00 3F 87 FF FF FF FF FF FF FF FF FF FF FF
66E0h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
66F0h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00
6700h: 00 00 00 00 00 00 00 00 00 00 00 00 00 00

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generated signal (a 'needle pulse' with a repetition rate of 25 Hz) can be used to reset the counters and thus synchronise the entire process to an external system. The trick here is to have the oscillator run slightly slower, so the final bit of line 625 or the first bit of line 1 is present at the outputs when the next external reset occurs. A trimmer capacitor (C1) is added to the oscillator for this purpose, and it can be adjusted as necessary. The current consumption of the finished circuit is approximately 25 mA.

Table 1 lists the principal addresses and data for the synchronisation signal. The data for the first field and the equalisation pulses are contained in lines 00 through 49 (all

addresses are shown in hexadecimal form). In addresses 50 through 135F, identical data appear in each group of 16 bytes. The data for the equalisation pulses and the second field pulse can be seen at addresses 1360 through 13DF. The data for addresses 13E0 through 26DF are again identical for each group of 16 bytes. No data are used from address 2710 to the first address of the second table, so all of these locations are set to '0'. Here only the first following nibble is set to '1', in case it is desired to have the counters continue to count. This causes the level to remain High until line 1 starts again when the counters are reset.

Table 2 is primarily intended to serve as an example that shows where relevant video information and the colour-burst data should be located. The arrangement of Table 2 is similar to that of Table 1, although here the nature of the signal is different, and we show somewhat more of the full table. This is primarily done to indicate the addresses where colour-burst data should be placed with **no** video data. Pay careful attention to the address numbers if you want to copy this table.

Table 3 shows the most important timing specifications for the synchronisation signals, alongside the timing data for this

Table 3

	CCIR (PAL)	sync-generator
Line period	64 μ s	64 μ s
Front porch	1.5 $\pm$ 0.3 μ s	1.5 μ s
Line sync. width	4.7 $\pm$ 0.2 μ s	4.5 μ s
Back porch	5.8 $\pm$ 0.2 μ s	6.0 μ s
Start line to burst	5.6 $\pm$ 0.1 μ s	5.0 μ s
Burst duration	2.25 $\pm$ 0.23 μ s	3.5 μ s
Line blanking	12 $\pm$ 0.3 μ s	12 μ s
Field period	20 ms	20 ms
Field blanking	1.6 ms	1.676 ms
Eq. puls width	2.35 $\pm$ 0.1 μ s	2.5 μ s
Duration pre/post-eq.	160 μ s	160 μ s
Field sync. width	160 μ s	160 μ s
Interval in field sync.	27.3 $\pm$ 0.1 μ s	27.5 μ s

circuit. Bear in mind that one bit represents 0.5 μ s. One final remark: the EPROM content can be downloaded as file number **024071-21** from the Free Downloads page at www.elektor-electronics.co.uk.